OIPE IAP59
JAN 20 2006
PATENT & TRADEMARK OFFICE

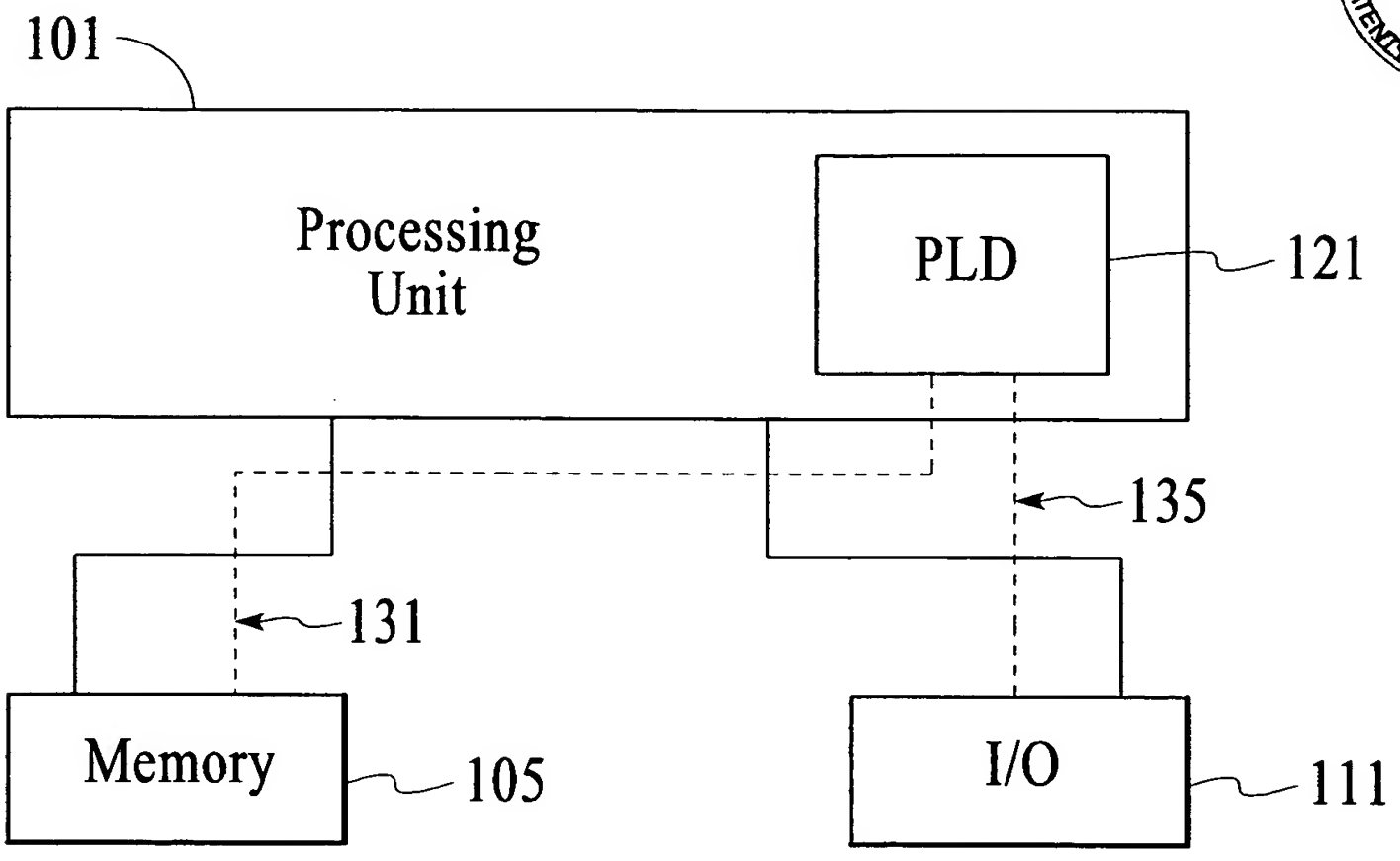


FIG.1

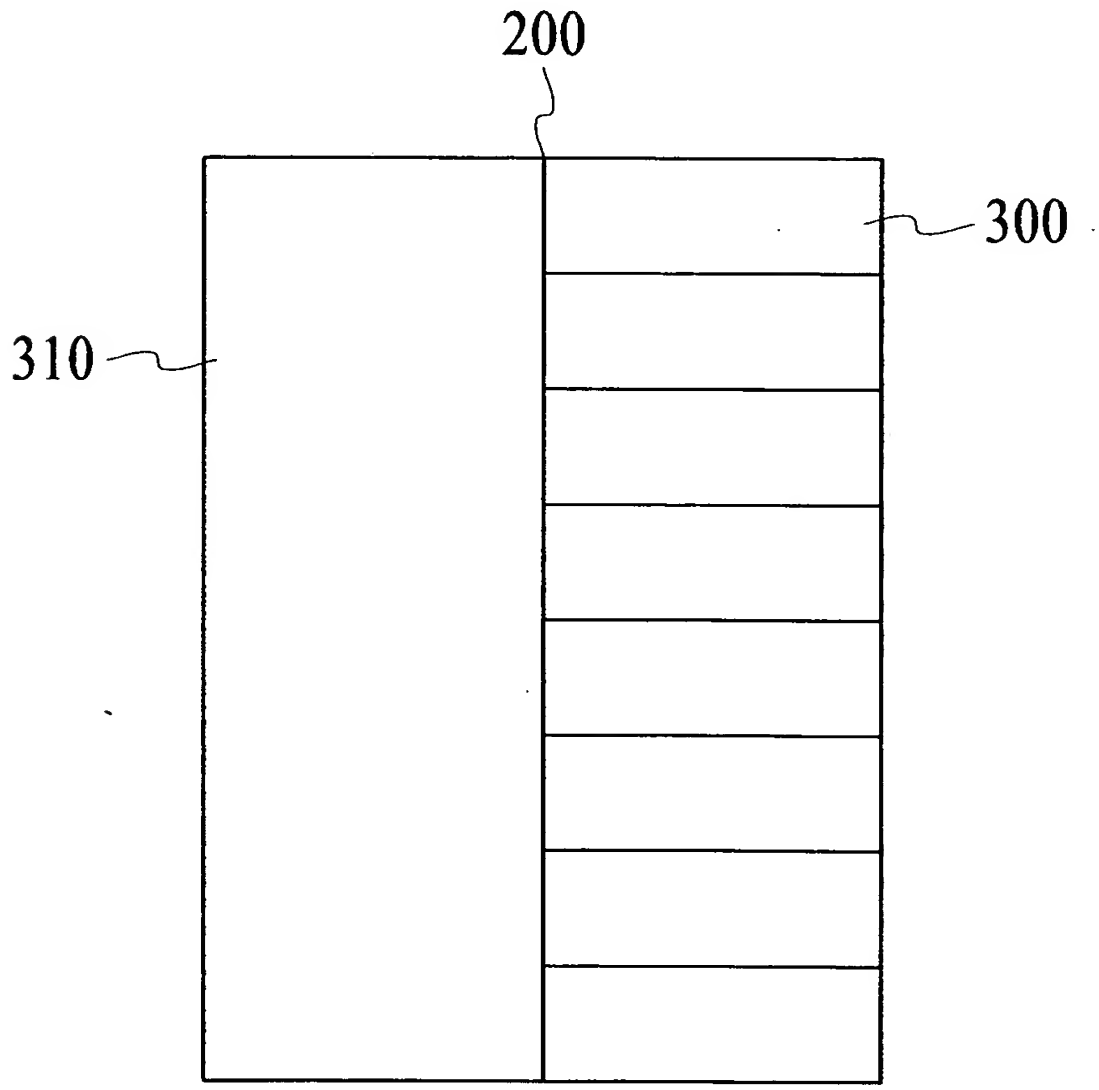


FIG.3

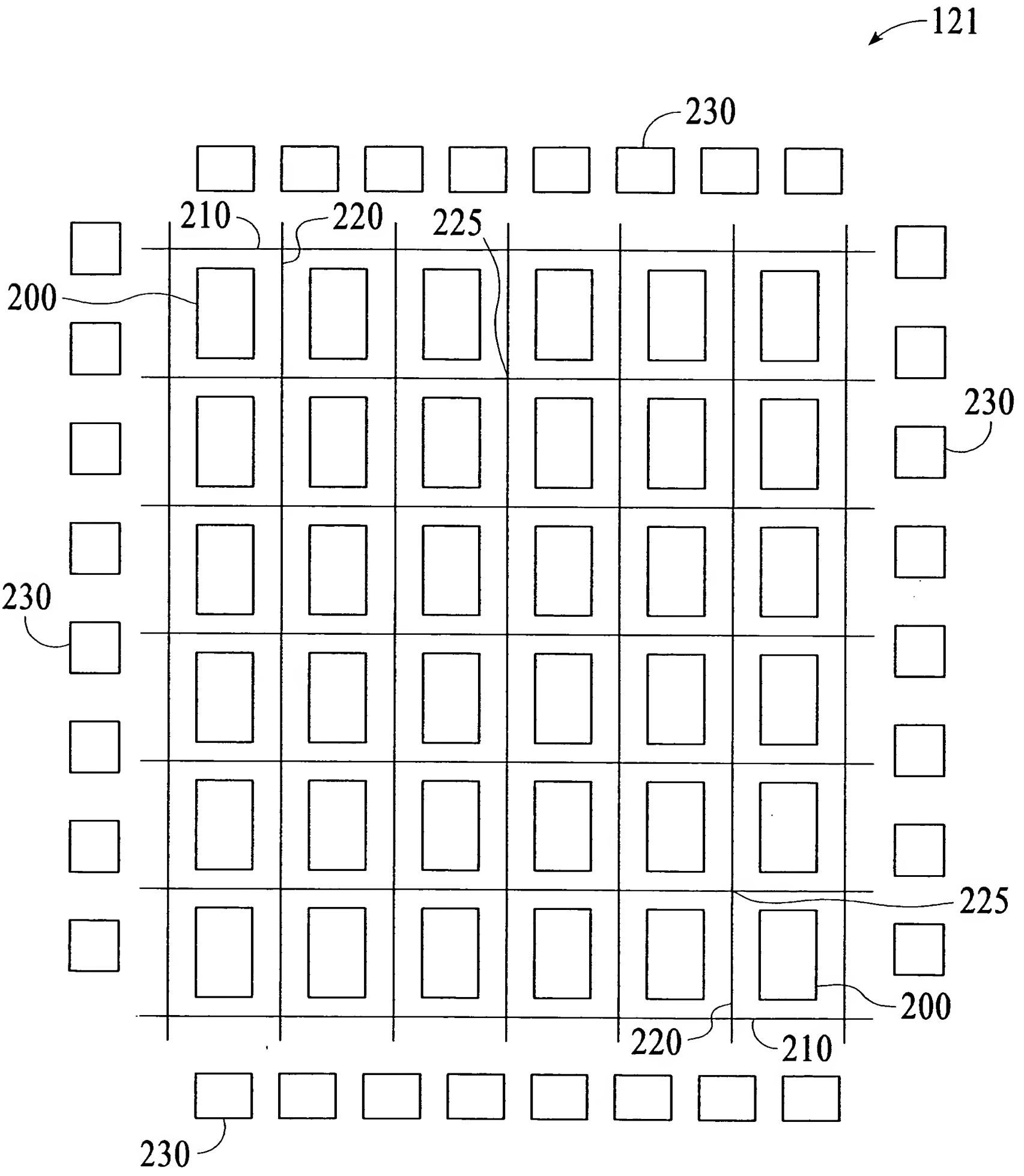


FIG.2

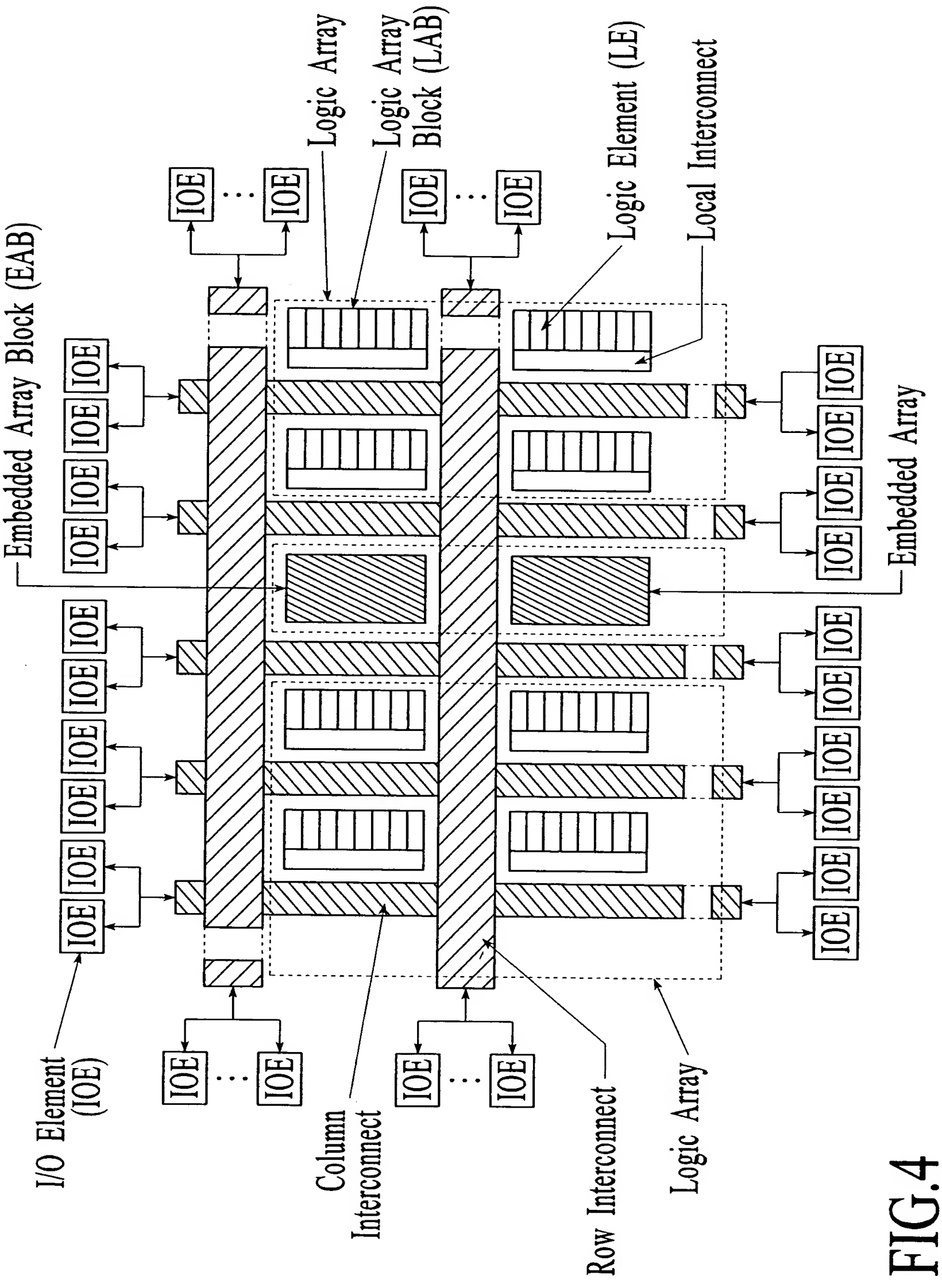
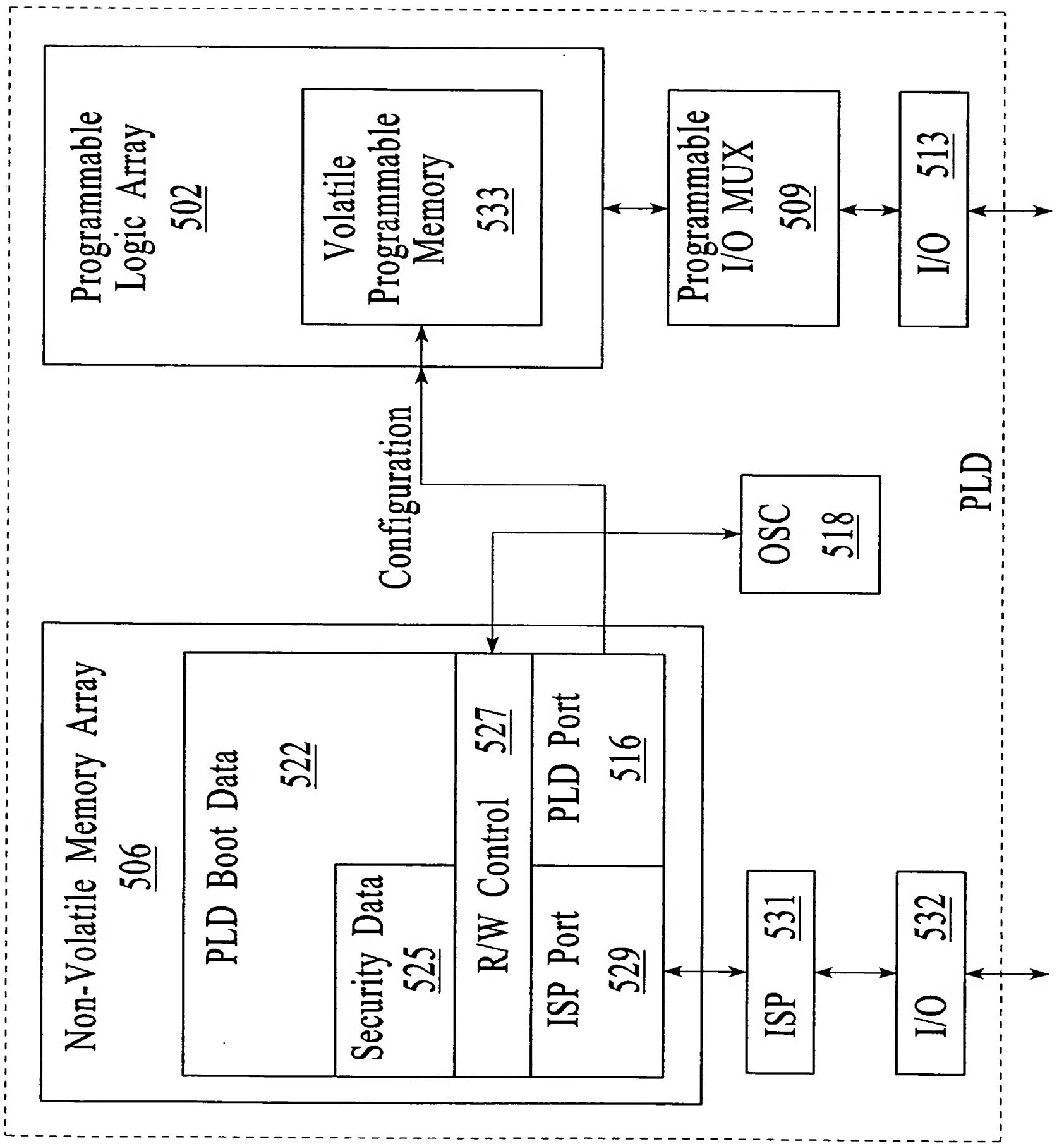

Logic Array
Logic Array Block (LAB)
Logic Element (LE)
Local Interconnect
Embedded Array Block (EAB)
Embedded Array
IOE
I/O Element (IOE)
Column Interconnect
Row Interconnect
Logic Array

FIG.4

FIG.5


PLD
Programmable Logic Array 502
Volatile Programmable Memory 533
Programmable I/O MUX 509
I/O 513
Configuration
OSC 518
Non-Volatile Memory Array 506
PLD Boot Data 522
Security Data 525
R/W Control 527
PLD Port 516
ISP Port 529
ISP 531
I/O 532

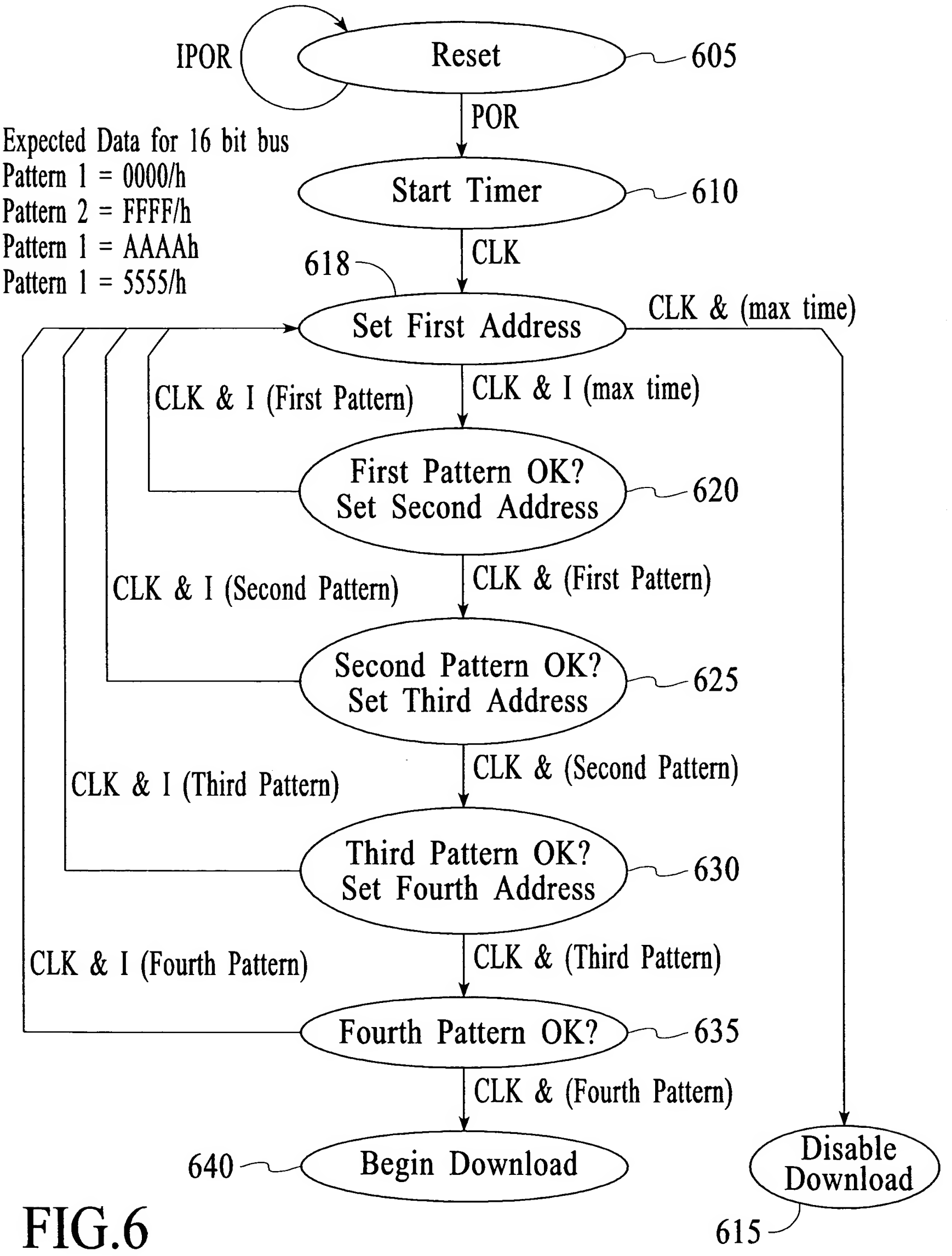

IPOR
Reset
605
POR
Expected Data for 16 bit bus
Pattern 1 = 0000/h
Pattern 2 = FFFF/h
Pattern 1 = AAAAh
Pattern 1 = 5555/h
Start Timer
610
CLK
618
Set First Address
CLK & (max time)
CLK & I (First Pattern)
CLK & I (max time)
First Pattern OK?
Set Second Address
620
CLK & I (Second Pattern)
CLK & (First Pattern)
Second Pattern OK?
Set Third Address
625
CLK & I (Third Pattern)
CLK & (Second Pattern)
Third Pattern OK?
Set Fourth Address
630
CLK & I (Fourth Pattern)
CLK & (Third Pattern)
Fourth Pattern OK?
635
CLK & (Fourth Pattern)
640
Begin Download
Disable
Download
615

FIG.6

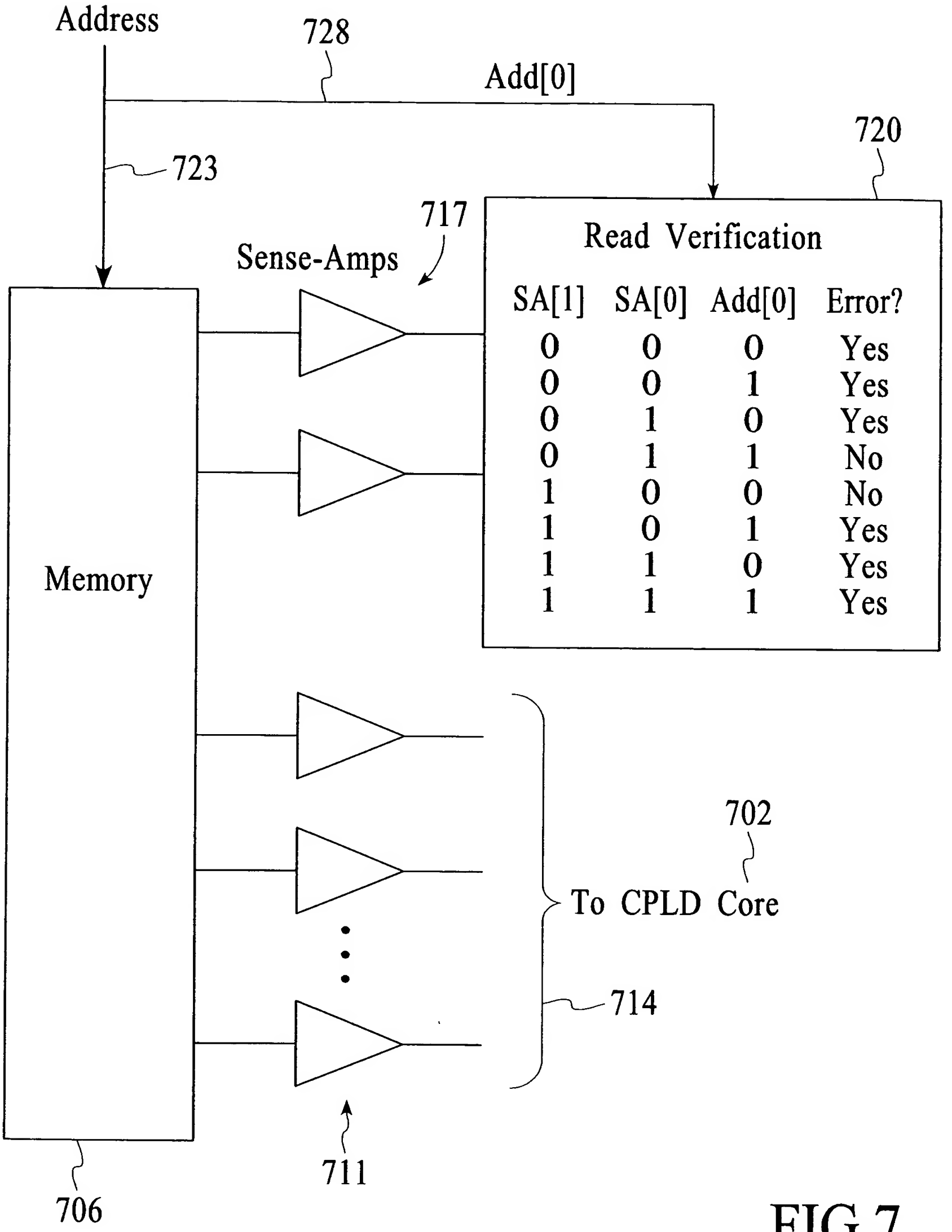

Address
728
Add[0]
720
723
717
Sense-Amps
Read Verification
SA[1] SA[0] Add[0] Error?
0 0 0 Yes
0 0 1 Yes
0 1 0 Yes
0 1 1 No
1 0 0 No
1 0 1 Yes
1 1 0 Yes
1 1 1 Yes
Memory
702
To CPLD Core
714
711
706

FIG.7